BROAD BAND RECEIVER DESIGN ON FPGA

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ABSTRACT

In this paper, we present a new receiver architecture, which is motivated by optimum detection of Amplitude Shift Keying (ASK) signals in the presence of Tikhonov-distributed residual phase error due to the phase-locked loop (PLL)-aided phase tracking scheme. And a computationally-efficient(C-E) receiver architecture is proposed to reduce the receiver architecture. Performances on AWGN and fading channels are evaluated by bit error rate (BER). The simulations show that BER performances follow those of the optimum receiver over a wide range of signal-to-noise ratio (SNR), while outperforming a standard coherent receiver operating in the presence of residual phase error by more than 2 dB. And by using System Generator, the C-E receiver architecture is implemented on Field-Programmable Gate Array (FPGA) under AWGN channel, which follows the simulation results.

Keywords: ASK, AWGN , BER, FPGA, C-E RECEIVER, PLL.

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1. INTRODUCTION:

In recent years, the Broadband Communication Systems like 3G/4G and WiMAX gain much more attention because of the high data rate transmission need in the wireless communication. High data rate modulation schemes, like Amplitude Switch Keying (ASK) have been widely used in Broadband Communication Systems. And this trend also provides challenges to the hardware design to support the high data rate transmitter and receiver with less complexity. However, because the fast-changing wireless channel environments can cause the serious phase and amplitude impairment to the information signals, even when pilot signal is used, the residual estimation error is still significant and changes fast. In this paper, we consider the industry trend by using partially coherent detection scheme because of the low complexity of receiver architecture design. With the aid of pilot signal and the Phase-locked Loop (PLL), which is widely used in industry, we design our receiver architecture accordingly.

Although the pilot signals and PLL can help to estimate the channel state information (CSI) with good accuracy, the residual phase estimation error is still un negligible, sometimes even quite significant when certain PLL is in use. By using the PLL, the residual phase estimation error obeys the Tikhonov distribution. We thus use this known probability density function (PDF) to reach the optimum partially coherent receiver architecture for QAM signals by using the maximum a posteriori probability (MAP) decision criterion. Here in this article, we consider the discrete memory less channel case and use the symbol-by-symbol detection technique (assume phase error changes fast enough) to get the close-form receiver structure. And this can be considered as the worst case channel scenario.

However, because of the high complexity of the optimum receiver, which may cause the hardware implementation difficulty, we propose a new computationally efficient (C-E) receiver architecture, which is more suitable for the hardware implementation by avoiding the Bessel function calculation.

2.1 BROADBAND RECEIVER:

A broadband receiver exhibiting reduced interference to a frequency counter caused by a local oscillator. The broadband receiver is arranged for detecting a radio signal of strong

reception intensity and receiving the radio signal, and in a specific configuration includes: a reception system including an antenna for receiving the radio signal, a local oscillator for outputting a local oscillation signal, a frequency mixer for converting the radio signal to an intermediate frequency, and a demodulator for demodulating the intermediate frequency;.

Frequency counter for measuring the frequency of a radio signal having strong reception intensity; a control section for controlling the oscillation frequency of the local oscillator in such a manner that the radio signal having a strong reception intensity is demodulated by the reception system; and a local oscillator halting section for halting the oscillation of the local oscillator during the measurement of the frequency of the radio signal by the frequency counter.A broadband receiver for detecting a radio signal of strong reception intensity and receiving said radio signal, comprising:

(a) a reception system including an antenna for receiving said radio signal, a local oscillator for outputting a local oscillation signal, a frequency mixer for converting said radio signal to an intermediate frequency by means of the local oscillation signal output by said local oscillator, and a demodulator for demodulating the intermediate frequency output by said frequency mixer;

(b) a first frequency counter set to a long cycle for measuring the frequency of a radio signal having strong reception intensity; a second frequency counter set to a short cycle for judging whether or not the frequency of said radio signal is stable; and a control section for controlling the oscillation frequency of said local oscillator in such a manner that said radio signal having a strong reception intensity is demodulated by said reception system; wherein said first frequency counter and said second frequency counter are activated simultaneously when measuring the frequency of said radio signal, the measurement of said radio frequency by said first frequency counter is continued if it is judged by said second frequency counter that the frequency of said radio signal is stable, and the measurement of said radio frequency by said first frequency counter is interrupted if it is judged by said second frequency counter that the frequency of said radio signal is not stable.

2.2 BROADBAND RECEIVER INVENTION:

In one aspect, the invention relates to a broadband receiver for detecting a radio signal of strong reception intensity and receiving the radio signal, comprising: a reception system including an antenna for receiving the radio signal, a local oscillator for outputting a local oscillation signal, a frequency mixer for converting the radio signal to an intermediate frequency by means of the local oscillation signal output by the local oscillator, and a demodulator for demodulating the intermediate frequency output by the frequency mixer; a frequency counter for measuring the frequency of a radio signal having strong reception intensity; a control section for controlling the oscillation frequency of the local oscillator in such a manner that the radio signal having a strong reception intensity is demodulated by the reception system; and a local oscillator halting section for halting the oscillation of the local oscillator during the measurement of the frequency of the radio signal by the frequency counter.

By halting the oscillation of the local oscillator while the frequency counter is measuring the frequency of the radio signal, it is possible to reduce the interference caused to the frequency counter by the local oscillator. In another aspect, the invention relates to a broadband receiver for detecting a radio signal of strong reception intensity and receiving the radio signal, comprising: a reception system including an antenna for receiving the radio signal, a local oscillator for outputting a local oscillation signal.

Frequency mixer for converting the radio signal to an intermediate frequency by means of the local oscillation signal output by the local oscillator, and a demodulator for demodulating the intermediate frequency output by the frequency mixer; a frequency counter for measuring the frequency of a radio signal having strong reception intensity; a control section for controlling the oscillation frequency of the local oscillator in such a manner that the radio signal having a strong reception intensity is demodulated by the reception system.

Storage section for storing radio frequencies that are unwanted for reception; wherein the control section disregards the detection of a radio signal having a strong reception intensity, and performs detection of a new radio signal having a strong reception intensity, if the frequency of the radio signal measured by the frequency counter coincides with an unwanted radio frequency

stored in the storage section or a frequency in the vicinity of same. By means of this construction and arrangement, it is possible to avoid detection and reception of previously determined unwanted radio waves.

In a further aspect, the invention relates to a broadband receiver for detecting a radio signal of strong reception intensity and receiving the radio signal, comprising: a reception system including an antenna for receiving the radio signal, a local oscillator for outputting a local oscillation signal, a frequency mixer for converting the radio signal to an intermediate frequency by means of the local oscillation signal output by the local oscillator, and a demodulator for demodulating the intermediate frequency output by the frequency mixer; a frequency counter for measuring the frequency of a radio signal having strong reception intensity.

Control section for controlling the oscillation frequency of the local oscillator in such a manner that the radio signal having a strong reception intensity is demodulated by the reception system; and a storage section for storing radio frequencies that have been received in the past; wherein the control section disregards the detection of a radio signal having a strong reception intensity, and performs detection of a new radio signal having a strong reception intensity, if the frequency of the radio signal measured by the frequency counter coincides with a previously received radio frequency stored in the storage section or a frequency in the vicinity of same.

By means of this construction and arrangement, it is possible to eliminate problems wherein a radio signal of the same frequency is detected and received repeatedly. In yet another aspect, the invention relates to a broadband receiver for detecting a radio signal of strong reception intensity and receiving the radio signal, comprising: a reception system including an antenna for receiving the radio signal, a local oscillator for outputting a local oscillation signal, a frequency mixer for converting the radio signal to an intermediate frequency by means of the local oscillation signal output by the local oscillator, and a demodulator for demodulating the intermediate frequency output by the frequency mixer; a first frequency counter set to a long cycle for measuring the frequency of a radio signal having strong reception intensity; a second frequency counter set to a short cycle for judging whether or not the frequency of the radio signal is stable; and a control section for controlling the oscillation frequency of the local oscillator in

such a manner that the radio signal having a strong reception intensity is demodulated by the reception system; wherein the first frequency counter and the second frequency counter are activated simultaneously when measuring the frequency of the radio signal, the measurement of the radio frequency by the first frequency counter is continued if it is judged by the second frequency counter that the frequency of the radio signal is stable, and the measurement of the radio frequency by the first frequency counter is interrupted if it is judged by the second frequency counter that the frequency of the radio signal is not stable. By means of this construction and arrangement, it is possible to perform highly accurate frequency measurement in a short period of time.

2.3 BROAD BAND TYPES:

Broadband includes several high-speed transmission technologies such as:

1.Digital Subscriber Line (DSL)

2.Cable Modem

3.Fiber

4.Wireless

5.Satellite

6.Broadband over Power lines (BPL)

3.AMPLITUDE SHIFT KEYING (ASK):

Amplitude-shift keying (**ASK**) is a form of modulation that represents digital data as variations in the amplitude of a carrier wave. The amplitude of an analog carrier signal varies in accordance with the bit stream (modulating signal), keeping frequency and phase constant. The level of amplitude can be used to represent binary logic 0s and 1s. We can think of a carrier signal as an ON or OFF switch. In the modulated signal, logic 0 is represented by the absence of a carrier, thus giving OFF/ON keying operation and hence the name given. Like AM, ASK is also linear and sensitive to atmospheric noise, distortions, propagation conditions on different routes in PSTN, etc. Both ASK modulation and demodulation processes are relatively inexpensive. The ASK technique is also commonly used to transmit digital data over optical fiber. For LED transmitters, binary 1 is represented by a short pulse of light and binary 0 by the absence of light.

Laser transmitters normally have a fixed "bias" current that causes the device to emit a low light level. This low level represents binary 0, while a higher-amplitude light wave represents binary 1.

4. INTRODUCTION TO FPGA KIT:

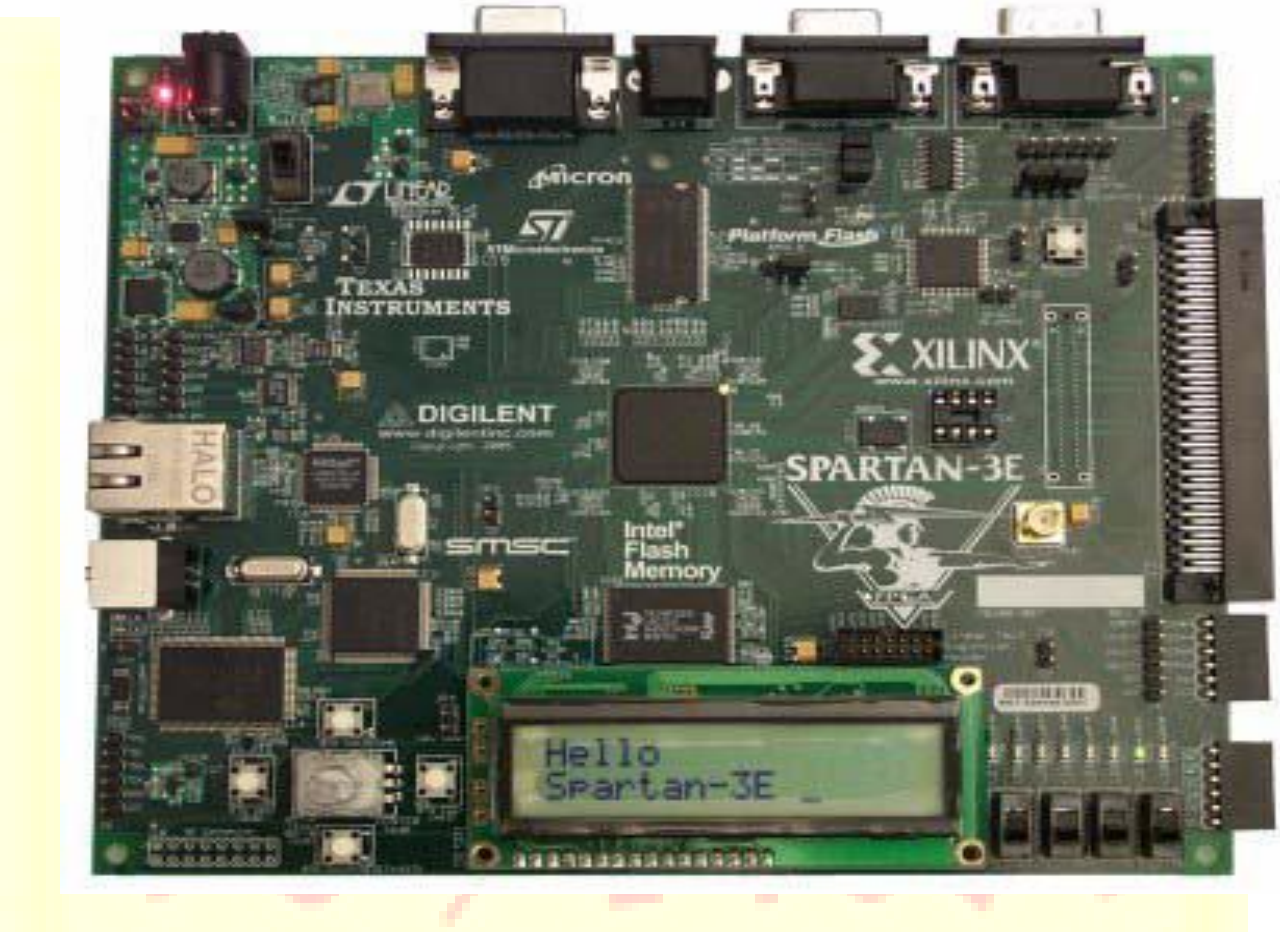

FIGURE:1 Spartan-3E FPGA Features and Embedded Processing Functions

The Spartan-3E Starter Kit board highlights the unique features of the Spartan-3E FPGA family and provides a convenient development board for embedded processing applications. The board highlights these features:

1.Spartan-3E specific features

2.Parallel NOR Flash configuration

3.MultiBoot FPGA configuration from Parallel NOR Flash PROM

4.SPI serial Flash configuration 5.Embedded development.

4.1 Setup:

Spartan-3 board with a RS-232 terminal connected to the serial port and configured for 57600 baud, with 8 data bits, no parity and no handshakes.

4.1.1 Creating the Project File in XPS:

The first step in this tutorial is using the Xilinx Platform Studio (XPS) to create a project file. XPS allows you to control the hardware and software development of the Micro Blaze system, and includes the following:

- An editor and a project management interface for creating and editing source code
- Software tool flow configuration options

You can use XPS to create the following files:

• Project Navigator project file that allows you to control the hardware implementation flow

• Microprocessor Hardware Specification (MHS) file

Note: For more information on the MHS file, refer to the "Microprocessor Hardware Specification (MHS)" chapter in the Platform Specification Format Reference Manual.

• Microprocessor Software Specification (MSS) file

Note: For more information on the MSS file, refer to the "Microprocessor Software Specification (MSS)" chapter in the Platform Specification Format Reference Manual...

XPS supports the software tool flows associated with these software specifications.

Additionally, you can use XPS to customize software libraries, drivers, and interrupt handlers, and to compile your programs.

4.1.2 Starting XPS:

• To open XPS, select Start → Programs → Xilinx Platform Studio 8.1i → Xilinx Platform Studio

• Select Base System Builder Wizard (BSB) to open the Create New Project Using BSB Wizard dialog box shownin Figure 1.

• Click Ok.

• Use the Project File Browse button to browse to the folder you want as your project directory.

• Click Open to create the system.xmp file then Save.

• Click Ok to start the BSB wizard.

Note: XPS does not support directory or project names which include spaces.

4.1.3 MHS and MPD Files:

The next step in the tutorial is defining the embedded system hardware with the Microprocessor Hardware Specification (MHS) and Microprocessor Peripheral Description (MPD) files.

4.1.4 MHS File:

The Microprocessor Hardware Specification (MHS) file describes the following:

• Embedded processor: either the soft core MicroBlaze processor or the hard core PowerPC (only available in Virtex-II Pro and Virtex-4 FX devices)

• Peripherals and associated address spaces

• Buses

• Overall connectivity of the system

The MHS file is a readable text file that is an input to the Platform Generator (the hardware system building tool).Conceptually, the MHS file is a textual schematic of the embedded system. To instantiate a component in the MHS file, you must include information specific to the component.

4.1.5 MPD File:

Each system peripheral has a corresponding MPD file. The MPD file is the symbol of the embedded system peripheral to the MHS schematic of the embedded system. The MPD file contains all of the available ports and hardware parameters for a peripheral. The tutorial MPD file is located in the following directory:

$XILINX_EDK/hw/XilinxProcessorIPLib/pcores/<peripheral name>/data

Note: For more information on the MPD and MHS files, refer to the "Microprocessor Peripheral Description (MPD)" and "Microprocessor Hardware Specification (MHS)" chapters in the Embedded System Tools Guide.

EDK provides two methods for creating the MHS file. Base System Builder Wizard and the dd/Edit Cores Dialog assist you in building the processor system, which is defined in the MHS file. This tutorial illustrates the Base System Builder.Using the Base System Builder Wizard

Use the following steps to create the processor system:

• In the Base System Builder – Select "I would like to create a new design" then click Next.

• In the Base System Builder - Select Board Dialog select the following, as shown in Figure 2:

• Board Vendor: Xilinx

• Board Name: Spartan-3E

• Board Version: C, D.

To debug the design, follow these steps:In XPS select Deug-> XMD debug Options. The XMD Debug Options dialog box allows the user to specify the connections type and JTAG chain Definition . The connection types are available for MicroBlaze:

- Simulator – enables XMD to connect to the MicroBlaze ISS
- Hardware – enables XMD to connect to the MDM peripheral in the hardware
- Stub – enables XMD to connect to the JTAG UART or UART via XMDSTUB
- Virtual platform – enables a virtual (c model) to be used

Verify that Hardware is selected-→Select Save--→Select Debug -> Launch XMD

6. SIMULATION AND TEST RESULTS:

A. Simulation Results :The performance measures established in terms of bit error rate (BER) are evaluated through Matlab simulation on both additive white Gaussian noise (AWGN) and the fading channels. Two different QAM modulation schemes, 8- and 16- QAM constellations are explored via simulation.

We consider the performances of the optimum receiver, the C-E receiver, the coherent receivers in the presence of phase error and the BER performance bound. Surprisingly, the C-E receiver performs nearly as well as its optimum counterpart for a wide range of SNR values with the error rates less than 10¡2 (the range of interest for most practical scenarios). As expected, the 8-QAM case shows lower BER than its 16-QAM counterpart under the same phase error. Moreover, 8-QAM does demonstrate a more significant Improvement in its performance as compared with 16-QAM for the proposed receiver. The impact of different PLL (*BLTs* varies) has also been shown in the partially-coherent reception for 8-QAM signaling can offer an improvement of about 2 dB in performance when compared with a coherent receiver which does not compensate for the residual phase error (BLTs = 0:1).

This gain reduces to about 1 dB for 16-QAM. We explore different fading cases by changing the K-factor of the Rician distribution. Here, K=0 and K=0.5 cases have been examined to explore the impacts of different fading channels to the performance of our receiver architecture. Unfortunately, the proposed receiver architecture does not show noticeable performance improvement for K=0 case (Rayleigh channel), which can be seen from Fig. 6. For both 8- and 16-QAM modulation schemes, even with the perfect channel Estimation of ® the C-E receiver has almost the same BER performance as the coherent receiver which does not compensate for the residual phase error.This can be explained that the deep fading has more significant impact than phase error to the receiver. However, when Rician channel case is considered, our proposed C-E receiver architecture shows significant improvement as compared with the conventional coherent receiver. the BER performance of 8-QAM modulation by using different PLLs have been examined. For 8-QAM modulation,

The performance of C-E receiver has about 2.5dB improvement in the range of 10¡3¡10¡2 as compared with the coherent receiver by using PLL with *BLTs* = 0:1. When *BLTs* = 0:001, it still reveals about 1dB of improvement in performance. And it is also shown in the plots that the C-E receiver architecture can achieve more performance improvement at higher SNR for 8-QAM.

B. FPGA Implementation Test Results: In our prototype design, we choose Virtex-II Pro XC2VP30 from Xilinx, with 100MHz system clock, to support our receiver work on high speed up to 100Mbps. The prototype platform is realized under Mathworks' Simulink and Xilinx's System Generator. This platform offers a quick evaluation of implementation performance of the receiver design on hardware. Because of the complexity of the receiver design, the 16QAM receiver system platform design is a little too big to be implemented in one FPGA,so we implement the 8-QAM modulation scheme and test the receiver performance both on System Generator design and on FPGA platform. By testing the receiver platform both in Simulink and on FPGA board in AWGN chanel, we can clearly see that the receiver performs as well as it shows in the simulation. This means that when *Eb=N*0 is between 10¡12dB, the BER performance tested on FPGA board is in the range of 10¡3 ¡ 10¡2, which matches our simulation results

7. CONCLUSION: This paper uses a cell (pixel) network as the core of the architecture to implement segmentation with some degree of parallelism. An effort is made to integrate all the blocks used in the segmentation. They have implemented the different blocks in the architecture in such a way as to reduce the circuit area, minimum wire length and high layout regularity. These authors have the same segmentation architecture combined that with feature extraction block, pattern matching block to track moving objects in. They have interleaved these functions to adopt pipelining in the architecture to speed up the computation. More parallelism in the segmentation process can be introduced at the cost of increased hardware. The processor is designed such that more image processing techniques could be incorporated by putting additional functional blocks in the operator unit. The segmentation processor can then mimic an image processor at low cost hardware.

8. REFERENCES:

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